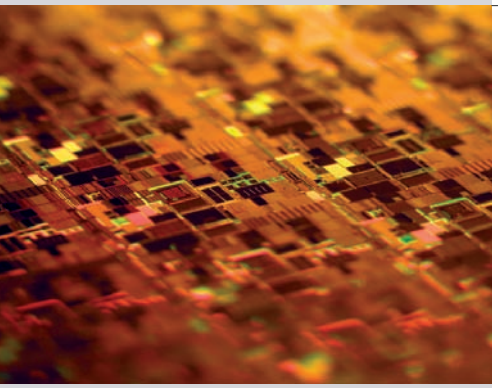
PROJECT RESULT

Technology platform for next-generation core CMOS process

MEDEA+

2TI03: Integration of 45 nm CMOS technology (FOREMOST)



European chipmakers define processing technology for 45 nm node devices

Mass-production capability in consumer electronics relies heavily on the performance and availability of the underlying microelectronics circuitry. With global chip production now moving fast to the 45 nm node, Europe needed to ensure it could mass produce semiconductors to this new world standard. The two-phase MEDEA+ FOREMOST project developed advanced process modules and chip architectures for full 45 nm node CMOS and 50 nm DRAM memory technologies in European 300 mm wafer-fabrication plants, boosting the reputation and position of Europe's chipmakers and their suppliers on the global market.

Market advantage in microelectronics systems depends upon continual reduction in package size allied with improved performance and lower power consumption. Current mass-production capabilities for CMOS logic and DRAM memory chips – the most common semiconductor devices – worldwide are mostly at the 65 nm node.

Global consumer-product manufacturers are therefore looking to the latest generation of devices using 45 nm node technology to deliver on market expectations of higher performance and smaller size. The MEDEA+ 2T103 FOREMOST project set out to ensure European chipmakers could meet rising market demand for 45 nm technology, enabling Europe to deliver the business and consumer products that the market expects.

Building on earlier results

FOREMOST built on the results achieved by the EU Sixth Framework Programme (FP6) NANOCMOS project, which carried out a first screening and demonstration of materials, device and interconnect architectures for such CMOS logic. It developed advanced process modules and transistor architectures, and integrated them into a complete process flow to prove full CMOS 45 nm production technology.

The project consortium included chipmakers, materials producers and suppliers, academia and equipment manufacturers. A particular focus came from semiconductor manufacturers Qimonda/Infineon in Dresden, Germany and the Crolles 2 Alliance of Freescale, NXP Semiconductors and STMicroelectronics in France, with the aim of developing world-class production standards at these centres.

The project targeted the 45 nm node for CMOS logic, DRAM and non-volatile flash memory, and promoted a synergy between the competences of Crolles, Dresden and STMicroelectronics Italy. Work was split into two phases:

1. The low power (LP) CMOS 45 nm platform and DRAM technology steps development and qualification; and
2. Integration of improved solutions into the main core LP technology and in full DRAM process integration.

Smooth transfer

Some 90 scientists were involved in Crolles initially – when both NXP and Freescale withdrew from the Alliance at the end of 2007, the other consortium partners made a major effort to adapt to this situation. The work in Crolles should lead to about 500 direct-production jobs after production ramp-up of 45 nm capability from 2010 on.

The level of development achieved in the

45 nm LP process has enabled a smooth transfer to the production stage, and to the finalisation of an even more highly integrated version – the CMOS 40 nm LP process. STMicroelectronics was one of the first manufacturers in the world to offer such 45 nm technology. And the 45 nm process developed in the first phase of FOREMOST has become the core process used worldwide for mobile phone devices.

Major companies in multimedia and mobile-phone development are expected to use STMicroelectronics-based 45/40 nm LP processes. There is also interest from consumer electronics groups for printers and set-top boxes, thanks to the lower cost of the process and its early availability.

The success of FOREMOST will also pave the way for the development of 32/28 nm node technologies, enabling certain project partners to join the worldwide IBM 32 nm CMOS foundation with promising chipmaking activity in Crolles and Dresden.

Pushing the envelope

Thanks to FOREMOST, CEA-LETI and Fraunhofer CNT have confirmed their positions as leading-edge research institutes in electron-beam direct writing (EBDW), applying advanced lithographic-writing techniques for 200 and 300 mm wafers in partnership with Vistec Electron Beam.

Moreover, CEA-LETI has pushed development of the back-end-of-the-line chip-flow process to become one of the most mature technologies to be established as a standard within STMicroelectronics. This process is now used by most major companies involved in interconnect development. CEA-LETI is playing an important research role in the IBM CMOS research consortium at Fishkill & Albany in the USA.

IBS has already made several qualification demonstrations of its PULSION plasma immersion ion-implantation system for major customers and a PULSION tool has been installed at CEA-LETI. Process results obtained in FOREMOST have enabled IBS to enter the microelectronics equipment market, in which potentially 20% of the low-energy implanters can be plasma immersion tools. IBS has thus widened its commercial network and extended it to the USA and Asia. Recent financial investments and a partnership deal with a big equipment manufacturer supported the building and sales of the first high productivity PULSION tools.

Tool-manufacturer partners have also benefited from the success of FOREMOST. For example both AIXTRON and ASM are now marketing new systems and tools to underpin the chip-fabrication process. And project participation has also enabled materials suppliers SAFC Hitech and Air Liquide to maintain their leadership positions through their precursor qualification conducted with the support of LMGP. UJF/LTM also anticipated advance gate-stack etching with narrow dimension control.

Safeguarding manufacturing

FOREMOST has enabled the key European players in semiconductor manufacturing to develop advanced 45 nm logic technologies in line with market expectations, thus safeguarding and boosting the position of Europe's chipmakers and their equipment and materials suppliers on the world market.

More than 80 papers were released during the project and 30 patents have been submitted. In addition, some 43 conference presentations were given around the world covering materials, plasma, chemistry, simulations, integration and devices.

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PARTNERS:

Air Liquide
AIXTRON
ASM France
ASM International (phase 1 only)
CEA-LETI
CNR-INFM-MDM
CNT
Freescale (phase 1 only)
IBS
IMEC (phase 1 only)
INPG-IMEP
Jordan Valley
LAHC Uni Savoie
LMGP
LTM-UJF
NCSR Demokritos (phase 1 only)
NXP Semiconductors (phase 1 only)
Qimonda
SAFC Hitech
STMicroelectronics
Vistec Electron Beam

PROJECT LEADER:

Jean-Louis Carbonero
STMicroelectronics

KEY PROJECT DATES:

Start: January 2006
End: June 2009

COUNTRIES INVOLVED:

Belgium (phase 1 only)
France
Germany
Greece (phase 1 only)
Israel
Italy
The Netherlands (phase 1 only)
United Kingdom

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MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon.